A DSP based Digitally Controlled Interleaved PFC Converter

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Abstract

A single DSP controlled two phase interleaved PFC converter is presented together with its digital control design and implementation. A simple, low cost method of sensing the switch current and implementing the current share control is illustrated. Details of the design are presented to show the simplification of the control implementation achieved through the use of a DSP. Finally, experimental results are provided to validate the performance of the digital implementation.

1. Introduction

Power Factor Correction (PFC) is an important aspect of power system design. While there are several approaches to achieve harmonic current reduction in low to medium power systems, for high power systems the traditional approach is a single stage boost converter operated in continuous conduction mode (CCM) [1]. In telecom/datacom 1kW rectifiers it is also common to parallel MOSFETs to reduce conduction losses.

The traditional control approach is to use a standard analog control integrated circuit (IC) which implements average current mode control (ACMC) and uses a multiplier [2] to achieve PFC. Since the output voltage of the boost converter must be above the peak of the line (typically 385V) the boost converter is followed by a dc-dc converter to produce the required regulated output or bus voltage.

Another well known technique is to operate the boost converter as a multi-phase or interleaved converter [3-4]. This technique has several advantages for high power systems. Since the power is processed by multiple converters the conduction losses for each converter are reduced. The MOSFET conduction losses, given by $I^2 R$, can dominate and so cutting the current in half (for two converters operating in parallel) will reduce the losses by a factor of four. In addition there are other power stage advantages to interleaving such as allowing smaller inductors with correspondingly higher ripple current, which has large signal advantages such as, reduced line current distortion, better transient response and less overshoot in a transient.

The complication of interleaving is mainly due to the control aspects. The system will typically require two control ICs as well as somewhat complex circuitry to force current sharing and ensure switching cycles are properly out of phase. Keeping multiplier reference currents similar requires extra circuitry. Additionally the analog control approach suffers from offsets and error terms that make a practical implementation difficult. For this reason although the benefits of interleaving are well known, and are used extensively in high current dc-dc converters, it has not been widely adopted in PFC systems.

However, with the advent of high performance DSP controllers new approaches to power converter control are possible. DSP based digital control removes many of the obstacles to interleaving PFC circuits. The low cost, high speed DSP controllers available today with integrated power electronic peripherals provide power supply designers with a new tool for flexible control design, high frequency operation, improved performance and increased system integration. Modern 32-bit DSPs, such as TMS320F2812 from Texas Instruments, highlighted by 150MHz CPU, 12-bit, 80nSec A/D converter, 32x32-bit multiplier, 32-bit timers and real-time code debugging capability deliver the flexibilities and benefits of digital control without compromising the performance[5-8]. The extra computing power of such processors allows the implementation of sophisticated nonlinear control algorithms, integrate multiple converter control into the same processor and optimize the total system cost.

This paper, therefore, presents the design and implementation of a single DSP controlled two phase interleaved PFC converter. Details of the design are presented to show how the use of a DSP simplifies the control implementation and allows for additional converter control. Finally, experimental results are provided to validate the performance of the digital implementation.

2. Power Stage

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The design of the PFC boost power stage is well known [1]. The main issues revolve around the semiconductor selection and magnetics design. The boost diode in a high power CCM design operates under severe conditions. Operating a converter with less current in the diode at turn-off significantly improves both stress on the diode and EMI. The interleaved approach allows us to run much larger ripple current in the inductors thereby allowing less current in the diode at the instant of turn-off. Although high ripple current usually has the disadvantage of contributing to increase filter requirements and higher peak current stress, interleaving alleviates these disadvantages. The individual channels will have lower peak currents than an equivalent single stage and ripple current cancellation will reduce the negative impact on filter requirements.

3. Digital Control Implementation for PFC Converter

A. DSP Interface to PFC Stage

Figure 3.1 shows the digitally controlled 2-stage interleaved power factor correction converter interfaced to the TMS320F2812 DSP.
As indicated in Figure 3.1, five signals are used to implement the control algorithm. These are, the input voltage *Vin*, the combined inductor current *Iin*, the switch currents Iq1, Iq2 and the dc bus voltage *Vbus*.

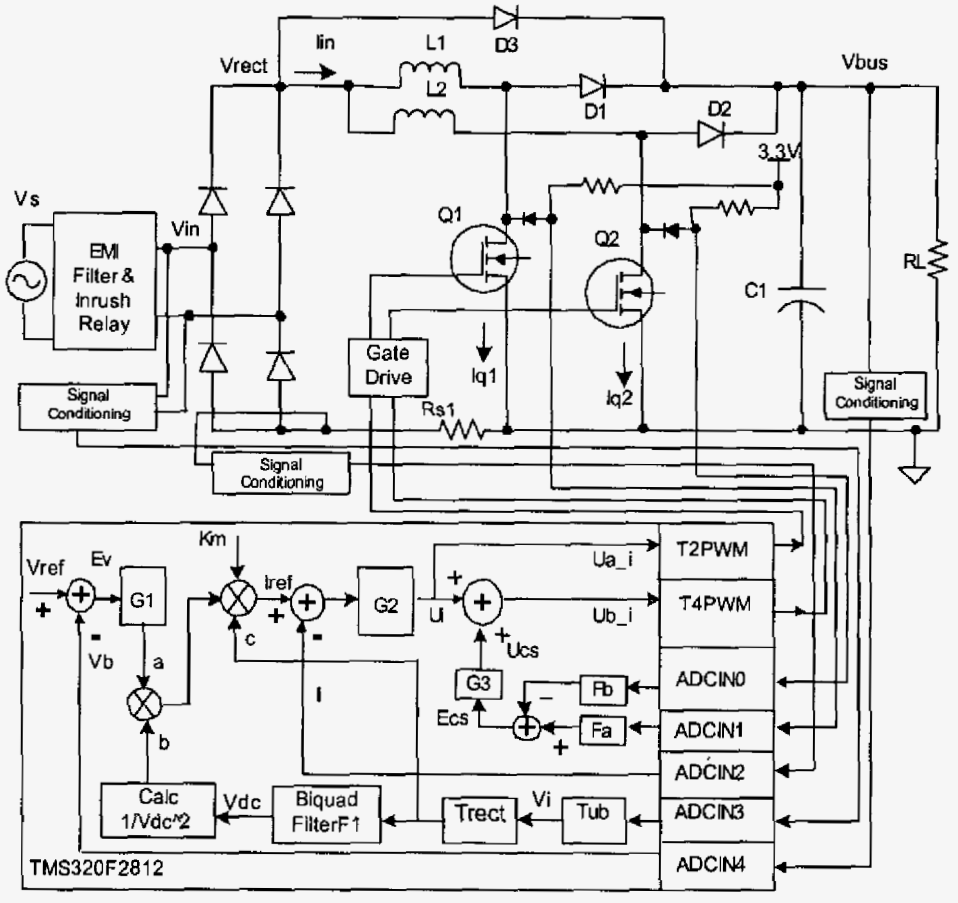


Figure 3.1 Digital Control of PFC stage

The converter is controlled by three feedback loops. The average output dc voltage is regulated by a slow response 'outer voltage loop' whereas the 'inner current loop' that shapes the input current is a much faster loop. A third 'current share loop' helps to maintain equal current through the two PFC MOSFETs.

B. PFC Stage Digital Sampling Loop Implementation

Figure 3.2 shows the PFC stage interleaved PWM waveform generation and the digital sampling loop implementation using the DSP on-chip peripherals. Three on-chip Timers T1, T2 and T4 are set up appropriately

and used to generate all the timing and the PWM outputs. Timer T1 generates a 200kHz asymmetric ramp waveform internal to the DSP and provides the main time base for interrupt generation, PWM outputs and triggering AD conversions. This PFC implementation is a part of a single DSP controlled AC-DC rectifier design where the DC-DC stage has a PWM frequency of 200kHz. This is achieved by setting the T1 ramp frequency as 200kHz. Timers T2 and T4, phase shifted by 180 deg with respect to each other and both synchronized to T1, generate 100kHz symmetric ramp waveforms internal to the DSP. These two timers are used to generate the two 100kHz interleaved PWM outputs for the PFC stage. These two PWM outputs are indicated in Figure 3.2 as T2PWM and T4PWM. The AD conversion for the five signals (*Vin, Vbus, Iq1, Iq2* and *Iin*) is triggered every time T1 counts up to its period value (peak of the T1 ramp). From the figure it is clear that this point is aligned to the peaks and valleys of T2 and T4. T2 and T4 are set up to generate dual edge modulated PWM outputs, T2PWM and T4PWM respectively. This choice of ADC start of conversion (ADCSOC at the peak of T1 ramp), therefore, ensures that the inductor current is sampled at the middle of the ON pulse of the PWM outputs in order to implement an average current mode control loop for the PFC converter. As soon as these signal conversions are complete, the ADC module is set up to generate an interrupt and in the interrupt service routine (ADC ISR), the user software reads the converted values from the ADC result registers. In Figure 3.2, the time difference between the start of AD conversion and the start of the subsequent ADC ISR is indicated as Tad. This time includes the total AD conversion time for the five signals plus the processor interrupt latency. Since T1 runs at 200kHz, these signal conversions are repeated at this rate. However, these signals are not used for control output calculation every time a new value is available. These are used for their respective control calculation only at a rate sufficient for achieving the individual control loop bandwidth (BW). For example, in this implementation the PFC current loop has the highest bandwidth among all three control loops. Therefore, the current loop controller calculation is performed at every other ISR i.e., at a rate of 100kHz. The reason for the 200kHz AD conversion rate and the ADC ISR execution rate is to satisfy the bandwidth requirement for a downstream dc-dc converter controlled by the same DSP controller and powered by this PFC stage.

For the PFC voltage loop, the control calculation is done in one out of every 200 ISRs, implying a voltage controller execution rate of 1kHz. For the current share loop, the controller execution rate is chosen as 100Hz because of its slowest bandwidth requirement. Also, the input to the current share controller is generated from the switch currents Iq1 and Iq2 by first saving these values at 50kHz rate (1 out of every 4 ISR) and then calculating a moving average value, for each current, using a set of 16 such samples(filters Fa and Fb in Figure 3.1). The error between these two average values is used as input to the current share controller G3.

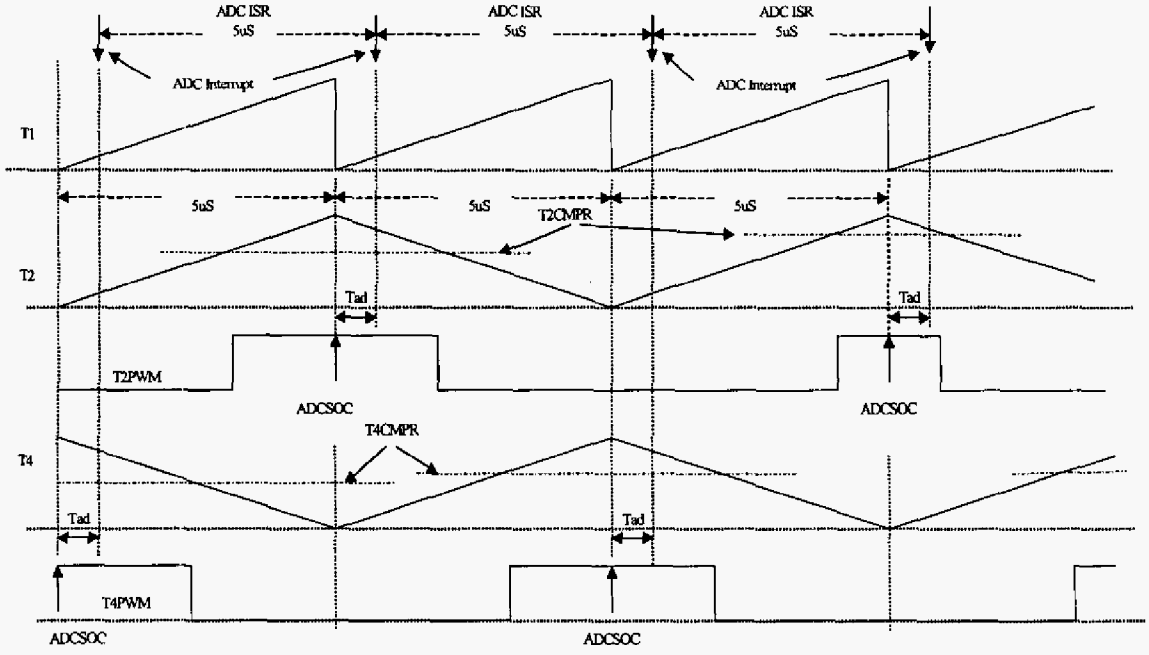


Figure 3.2 PFC stage PWM and Sampling Cycle

C. Module Current Sensing

While interleaving has many advantages, it also introduces challenges as well. One area that needs to be considered is current sensing of the individual channels. The typical current sense resistor location is in the return lead of the rectifier bridge (Figure 3.1, Rs1). However, while the signal at this point does give the total current in the system, it does not tell us where the current is coming from.

In order to control the individual modules current, switch current needs to be measured. Additionally, in order to get good response it is important that the A/D converters are driven with low output impedance. This would typically imply an amplifier buffer stage as is used in sensing the inductor current. Unfortunately due to the extremely high rising and falling edges of switch current, buffering this signal would require a high slew rate/ high bandwidth, relatively expensive amplifier.

A low cost method to measure switch current was developed and implemented. The circuit is shown in Figure 3.3. There are two identical circuits for each channel, with Channel A's circuit formed by diodes D1 through D3 with a resistor tied to a bias voltage. Diode D1 blocks the high voltage present on the drain of the MOSFET during its off-time. When the switch turns on the drain voltage falls, until the voltage falls below the bias voltage (3.3V), at this time, the voltage on the sensing node is equal to the voltage across the MOSFET, which in turn is equal to the product of switch current and the Rds,on of the MOSFET. There is a small error term associated with the bias current flowing into the MOSFET, however, this is small, and is the same in both switches. Since we are interested in the difference in currents, this term is insignificant. The larger error is due to differences in diode Vff. Again, the main purpose of the share loop is to maintain reasonable current sharing between the modules at maximum load. Diodes D2 and D3 are small schottky diodes whose purpose is to clamp any voltage spikes and protect the A/D inputs.

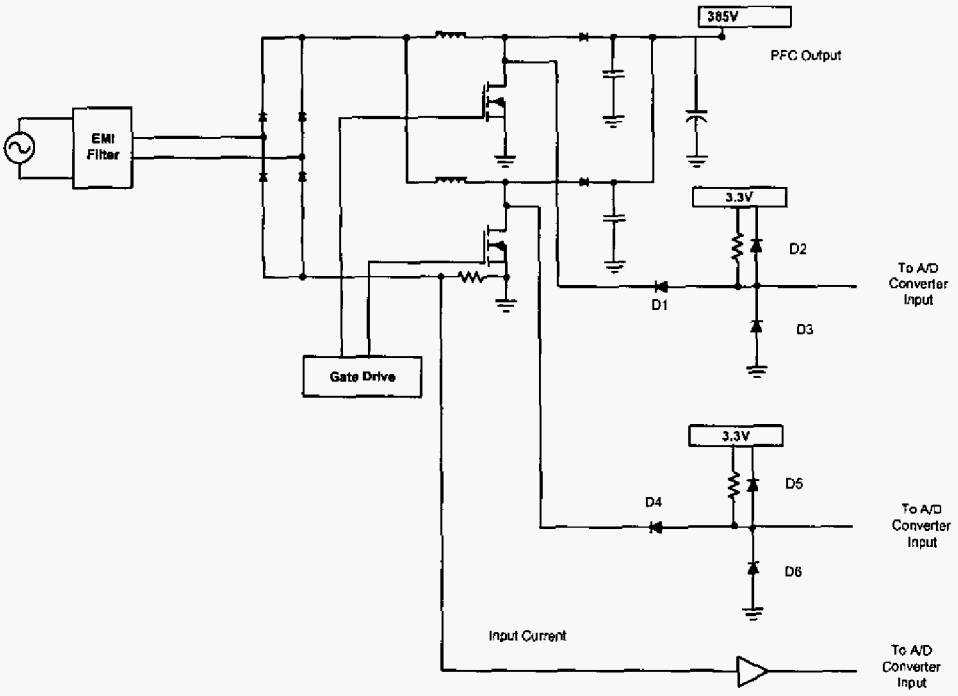


Figure 3.3 PFC stage module current sensing

Experimental results from the actual hardware are shown in Figure 4.2 verifying the modules sharing current. The circuit is simple, accurate and low cost. Each channel on time is shown in the waveform. The ramps in the lower portion of the traces are proportional to the actual switch current. It can be seen that the two channels conduct approximately the same amount of current.

A key advantage of the sampled nature of the system is the inherent noise rejection. Measuring switch current directly is often difficult due to the large current spikes at

the leading edge of the waveform. Also, at low duty cycles the sensing circuit can act as a peak detector. With digital control, and the sampling of signals, we have control over the sample instant. It is relatively easy to force sampling in the middle of the switch on-time. This provides a clean signal for even small pulse widths.

D. PFC Controller Design

The system parameters used in this design are:

- Output power Pout=1100W, Efficiency = 0.9
- Rated DC bus volt Vbus = 385V, Maximum DC bus volt Vdc_max = 400V
- PWM frequency fpwm=100kHz; Current loop sampling frequency fsi = 100kHz
- Boost Inductors L1, L2 = 200uH, Bus capacitor C1 = 810uF
- Maximum input voltage Vmax = 400V (peak), Minimum input voltage Vmin = 102V (peak)
- Voltage loop bandwidth fcv=10Hz, Current loop bandwidth fci=5kHz

In order to design the voltage and current controllers, the continuous time power stage model is first discretized with ZOH and samplers. Once this is available, a discrete-time compensator. i.e., a digital controller is designed directly in the z-domain using methods similar to the continuous-time frequency response methods. This has the advantage that the poles and zeros of the digital controllers are located directly in the z-plain, resulting in a better load transient response, as well as better phase margin and bandwidth for the closed loop control of the power converter.

The discrete-time transfer function Gid(z) of the current loop plant, including the ZOH, the sampler, the anti-aliasing filter Gf and the computation delay model Gdly is [9],

$$G_{id}(z) = Z\{\tfrac{1}{s}(1-e^{-sT}).G_f.G_{dly}.(K_s V_{bus}/sL)\}$$

where, Z denotes the z-transform of the function inside the parenthesis{}. Gf denotes the transfer function of a single pole low pass anti-aliasing filter. In this case the corner frequency of this LP filter is chosen as 30kHz. Gdly models the computation delay in the digital sampling loop. In this implementation the chosen sampling scheme results in a computation delay of half the sampling time, i.e., the computation delay is, Td = Tsi/2 where, Tsi (1/fsi) is the current loop sampling time. Now using MATLAB, this discrete time current loop plant model is computed as,

$$G_{id}(z) = 3.392(z^2 + 3.529z + 0.2852)/$$
$$(z^3 - 1.152z^2 + 0.1518z)$$

Where, the circuit parameters are chosen as, Vbus = 385V, L = 200uH and Tsi = 10.0uSec. The inductor current feedback factor in this case is Ks = 0.0413 as explained in [10]. For this plant model and the feedback factor, a suitable digital current controller that achieves a bandwidth of 5.8kHz, phase margin of 48.8 deg and gain margin of 10dB is designed in Matlab. Figure 3.4 shows the discrete current loop bode plot.

The resulting discrete current controller G2, computed from Matlab is

$$G2(z) = \frac{Ui}{Ei} = \frac{0.6507 - 0.8217z^{-1} + 0.2192z^{-2}}{1 - 1.1z^{-1} + 0.1z^{-2}}$$
$$\Rightarrow Ui(n) = 1.1\,Ui(n-1) - 0.1\,Ui(n-2) +$$
$$0.6507\,Ei(n) - 0.8217\,Ei(n-1) + 0.2192\,E(n-2)$$

Where, Ui is current controller output and Ei is the inductor current error signal.

The voltage loop plant transfer function in s-domain, including the feed forward term, has been explained in [10]. The discrete equivalent of this, including the ZOH and the sampler, is [9],

$$G_{vd}(z) = 3.959/(z-1)$$

Where the voltage loop sampling time is Tsv = 1.0mSec. The bus voltage feedback factor in this case is, Kd = 0.0025 as explained in [10]. For this plant model and the feedback factor, the digital voltage controller for a bandwidth of 10Hz is designed in Matlab as:

$$G1(z) = \frac{Uv}{Ev} = \frac{1.083 - 1.05z^{-1}}{1 - 1.829z^{-1} + 0.8287z^{-2}}$$
$$\Rightarrow Uv(n) = 1.829\,Uv(n-1) - 0.8287\,Uv(n-2) +$$
$$1.083\,Ev(n) - 1.05\,Ev(n-1)$$

Where, Uv is the voltage controller output and Ev is the dc bus voltage error.

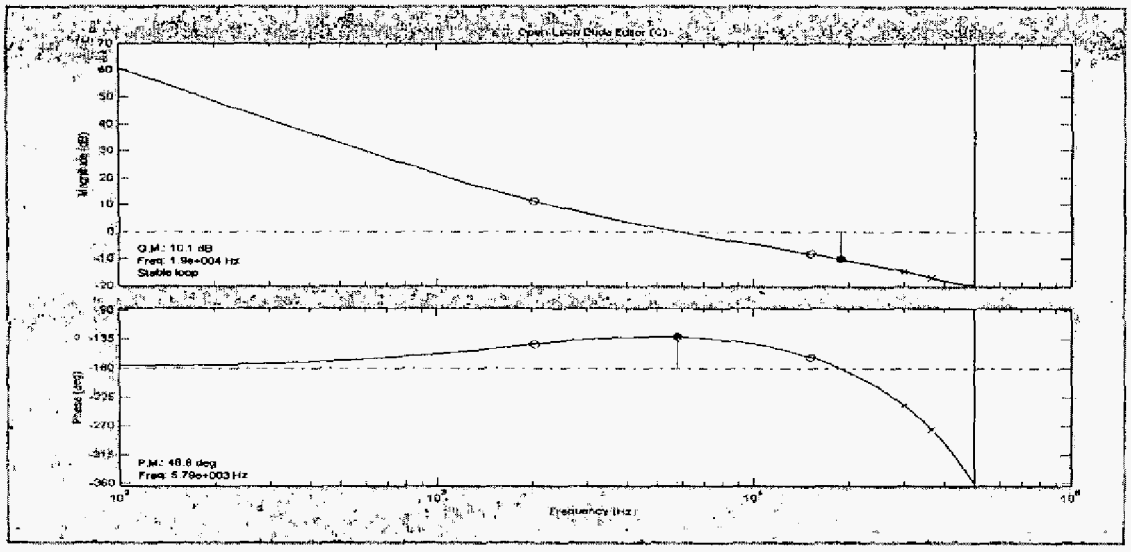
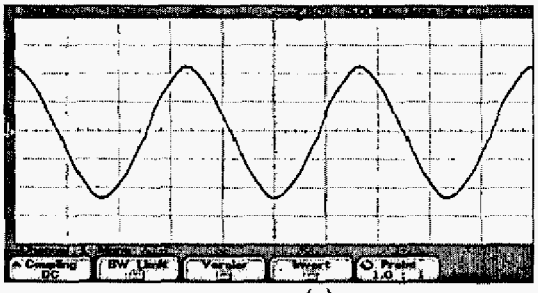


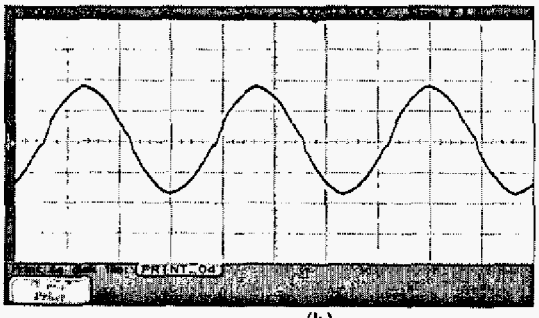
Figure 3.4 PFC stage discrete current loop bode plot (Matlab)

4. Experimental Results

A converter was designed and built using the techniques described. The performance of the digital PFC implementation was tested using this hardware. Figure 4.1 show the line currents for two different power outputs and for input voltage (Vin) of 120V RMS. Figure 4.1a is for output power of 860W and Figure 4.1b is for 580W.



(a)



(b)

Figure 4.1 PFC Stage Input Current

Figure 4.2 shows the current through each interleaved PFC switch. This is proportional to the voltages measured (by the current sense circuits) across the two MOSFETs. It can be seen that the two channels share current equally. Figure 4.3 shows the dc bus voltage transient response for a load step of 250W.

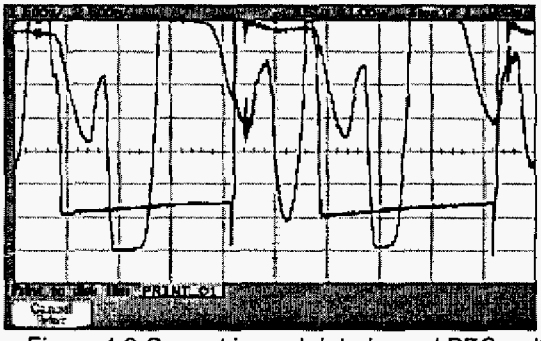


Figure 4.2 Current in each interleaved PFC switches

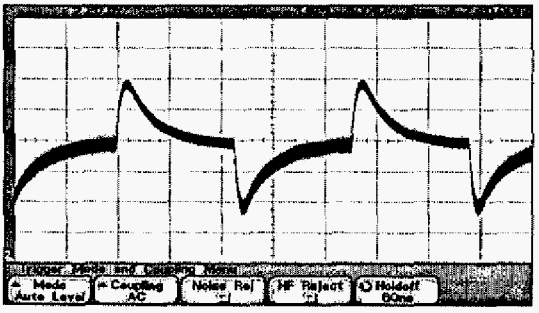


Figure 4.3 DC bus voltage transient response

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